PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE (Case No. 01-52)

First N	lamed Inventor: Antony Davies, Chienkuang Chenard Ling Wang										
Serial	No.: 10/006,559 FEB 1 1 2002 (C)) Group Unit: 2631									
Filed:	December 3, 2001) Examiner:										
Title:	Digital Phase Locked Loop with Phase Selector	,									
•	having Minimized Number of Phase Interpolators	RECEIVED									
A 4 C	Name and the Both of	FEB 1 5 2002									
	Commissioner for Patents ngton, D.C. 20231	Technology Center 2600									
Dear S	ir: TRANSMITTAL LE	TTER									
	In regard to the above identified application:										
	We are transmitting herewith the attached <u>Inf</u>	ormation Disclosure Statement and copies									
	of references cited; Form PTO-1449; and pos	tcard									
	2. With respect to additional fees:										
	X A. No additional fee is required.										
	B. Attached is a check in the amoun	t of \$									
	ž.										
- (B. CERTIFICATE OF MAILING UNDER 37 CFR § Transmittal Letter and the paper, as described in paragr United States Postal Service with sufficient postage as fill Commissioner for Patents, Washington, D.C. 20231 on the commission of	aph 1 hereinabove, are being deposited with the rst class mail in an envelope addressed to: Asst.									
	By Pho	ria H. Choi									

Monica H. Choi

Reg. No. 41,671

IN THE UNITED STATES PARENT AND TRADEMARK OFFICE (Case No. 01-52)

First N	amed Inventor:)	RECEIVED
	Antony Davies, Chienkuang Chen,)	FEB 1 5 2002
	and Ling Wang)	Technology Center 2600
Serial 1	No.: 10/006,559)	Group Unit: 2631
Filed:	December 3, 2001)	,
)	Examiner:
Title:	Digital Phase Locked Loop with Phase Selector)	
	having Minimized Number of Phase Interpolators)	
	•)	

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents Washington, D.C. 20231

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.97 - 1.98, the Applicants wish to make the following documents of record in the above-identified application. This Information Disclosure Statement is in compliance with the duty of candor as set forth in 37 C.F.R. § 1.56. Copies of the documents cited below are enclosed. These documents are also listed on the enclosed PTO Form 1449.

In the judgment of the undersigned, portions of the listed documents may be material to the patentability of the presently pending claim. However, the documents have not been reviewed in sufficient detail to make any other representation and, in particular, no representation is intended as to the relative importance of any portion of the documents. This

statement is not a representation that the listed documents have effective dates early enough to be "prior art" within the meaning of 35 U.S.C. § 102 or § 103.

List of Cited References

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FEB 1 5 2002

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Patent No.	<u>Title</u>	<u>Inventors</u>
5,604,775	Digital Phase Locked Loop having Coarse and Fine Stepsize Variable Delay Lines	Saitoh et al.
6,122,336	Digital Clock Recovery Circuit with Phase Interpolation	Anderson

II. Other

I.

Patents

<u>Title</u> <u>Publication Date</u> <u>Relevant Pages</u>

Clock Data Recovery Circuit Associated with Programmable Device Circuitry (PCT Publication No. WO 01/69837 A2)

09/20/2001

By:

Respectfully Submitted,

Date: February 5, 2002

Monica H. Choi

Reg. No. 41,671

Attorney for Applicant(s)
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CERTIFICATE OF MAILING

The undersigned hereby certifies that the foregoing INFORMATION DISCLOSURE STATEMENT is being deposited in the United States Postal Service, as first class mail, postage prepaid, in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231 on this 5th day of February, 2002.

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FEB 1 5 2002

Technology Center 2600

Monica H. Choi Reg. No. 41,671

FORM PTO-1449	U.S. Department of Commerce	Atty. Docket No.	Serial No.	
(Rev. 2-32)	Patent and Trademark Office	01-52	10/006,559	
	INFORMATION DISCLOSURE STATEMENT BY APPLICANT FEB 1 1 2002	Applicant: Antony Davies	et al.	
(i.	Jse several sheets if necessary TAADEMARK	Filing Date:	Group:	
	MAUG	December 3, 2001	2631	

U.S. PATENT DOCUMENTS

Examiner Initial			Docur	nent f	Numbe	er	·	Date	Name	Class	Subclass	Filing Date if Appropriate	
	. 5	6	0	4	7	7	5	02/18/97	Saitoh et al.	375	376	09/29/95	
	6	1	2	2	3	3	6	09/19/00	Anderson	375	371	09/11/97	

FOREIGN PATENT DOCUMENTS

																					Translation	
			ocun	ent N	lumb	er		Date	Country	Class	Subclass	Yes	No									
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc).

	PCT Publication No. WO 01/69837 A2, published September 20, 2001, Clock Data Recovery Circuit Associated with Programmable Logic Device Circuitry						
EXAMINER		DATE CONSIDERED					

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.